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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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			2191	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/533,506

Applicant(s)

THOMAS, BIJO

Examiner

Dean Phan

Art Unit

2191

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☐ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 May 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>05/02/05</u> | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Specification

The specification is objected to because there is no heading for each section. The Examiner suggests inserting section headings in the specification as provided in 37 CFR 1.77(b). For example, the heading "BACKGROUND OF THE INVENTION" should be inserted above paragraph [0001]. The heading "BRIEF DESCRIPTION OF THE DRAWINGS" should be inserted above paragraph [0012].

Drawings

The drawings are objected to because there is no label for each block in figure 1, 2, 3, and 4. These blocks need to have descriptive labels under 37 CFR 1.84(n) and 1.84(o). For example, "CPU1" may be used for the label of block 10a.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1, 3-4, 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Humphrey et al, (US Pat. 4,933,846).

As to claim 1, Humphrey et al. teach a data processing apparatus (abstract), comprising:

a plurality of data processing units (Abstract, figure 1 element "110", "112", "114", "116" and "118") each having an address output and a data input and/or output (Figure 1 element "102", "104", "106", "108", Column 4 line 15-24);

a plurality of memory units (Figure 3 element "204", "206", column 4 line 26-28), each having an address input and a data input and/or output (Figure 3 element "102", "104");

a switching unit (Figure 1 element "100", column 10 line 28-31) comprising:
first selectable connections between the data input and/or outputs of the processing units (Figure 1 element "102" "104", column 4 line 15-24) and selectable ones of the data input and/or outputs of the memory units (Figure 4a element "102" "104"),

second selectable connections from the address outputs of the processing units (Figure 1 element "102" "104", column 4 line 15-24) to the address inputs of selectable ones of the memory units (Figure 4a element "102" "104"),

a detection unit (Figure 4a element "280" "288") coupled to the address outputs of the processing units, arranged to detect repetitions of a period of an address pattern output by the at least one of the processing units (column 10 line 58-65),

a state holding element (Figure 4a element "284" "290") for controlling the first and second selectable connections, the state holding element (22a, 34) having an input coupled to the detection unit (Figure 4a element "283"), in order to switch the first and second selectable connections in response to the detection of a new one of said repetitions, so that identical addresses from the data processing units (*The physical addresses on each bank are identical*) alternately map to different ones of the memory units during successive repetitions.

As to claim 3, Humphrey et al. teach a data processing apparatus according to claim 1, wherein the detection unit comprises an address comparator (Figure 4a element "280" "288") arranged to detect whether addresses from the address output of a first one of the data processing units fall in a range of one or more addresses associated with the memory units (column 11 line 1-5), and to generate a detection signal indicating the new one of said repetitions (column 11 line 5-7) each time when one of the addresses from the address output of the first one of the data processing units has output addresses in said range a certain number of times.

As to claim 4, Humphrey et al. teach a data processing apparatus according to claim 3, wherein said certain number is one (column 11 line 1-5), and wherein said range is a subset of one or more of the addresses associated with the memory units (column 10 line 66-column 11 line 5; *There are 16 subsets in this disclosure's example*).

As to claim 9, Humphrey et al. teach a data processing unit according to claim 1, wherein said plurality of memory units comprises three or more memory units (column 9 line 63-65, column 10 line 66-column 11 line 5), the state holding element controlling the switching of the first and second selectable connections (Figure 4a element "284" "290"), so that identical addresses from the data processing units cyclically map to different ones of three or more of the memory units (column 9 line 63-65; *The physical addresses of each bank are identical*) during successive repetitions.

As to claim 10, Humphrey et al. teach a data processing unit according to claim 1, wherein the detection unit is arranged to perform the detection of repetitions involving repetition of read and/or write control signals from at least one of the processing units (column 11 line 8-24; *To read or to write data from bank 1 or 2, the chip selects must receive a signal from the decode circuitry*).

As to claim 11, Humphrey et al. teach a data processing method, the method comprising: detecting repetition of periods of access address patterns output from at least one of a plurality of processing units (Figure 4a element "280" "288", column 11

line 1-5); switching selectable connections between the data input and/or outputs of the processing units and the data input and/or outputs of selectable ones of a plurality of memory units (Figure 4a element ""284"" 290", column 11 line 5-7), so that a same addresses from at least one of the plurality of processing units alternately addresses a location in different ones of the memory units in dependence on the detection of said repetition (*The comparator generates a signal based on the uppermost bits, the physical addresses of each bank are identical*).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. (US Pat. No. 4,933,846), in the view of Nakagawa (U.S. Pat 4,939,636).

As to claim 2, Humphrey et al. teach a data processing apparatus according to claim 1. Humphrey et al. do not teach a criterion for detecting the new one of the repetitions is programmable under the control of a program executed by the apparatus. However, in the same field of data processing (column 1 line 14-16), Nakagawa et al.

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teach a criterion for detecting the new one of the repetitions is programmable under the control of a program executed by the apparatus (column 6 line 13-15). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Humphrey et al. and Nakagawa et al. because that would improve the flexibility of the switch unit.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. (US Pat. No. 4,933,846), in the view of Kobayashi et al. (U.S. Pat 4,583,163).

As to claim 5, Humphrey et al. teach a data processing apparatus according to claim 3 and the said certain number is greater than one. Humphrey et al. do not teach the apparatus comprising a counter for counting a counted number of the addresses from the address output of the first one of the data processing units in said range at least until said certain number. However, in the same field of data processing (Kobayashi abstract), Kobayashi teach the apparatus comprising a counter for counting a counted number of the addresses from the address output of the first one of the data processing units in said range at least until said certain number (column 4 line 29-34). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Humphrey et al. and Kobayashi et al. because that would be

"... capable of transferring data whose address is larger than a maximum address of a plurality of memory blocks constituting a main memory, even if the maximum memory address

of the main memory is not set in an end address register."

(Column 2 line 20-25)

Claim 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Humphrey et al. (US Pat. No# 4,933,846), in the view of Sukegawa et al. (U.S. Pat 5,673,383).

As to claim 6, Humphrey et al. teach a data processing apparatus according to claim 1. Humphrey et al. do not teach the detection unit comprises an access memory for the at least one of the data processing units the access memory. However, in the same field of memory management (Sukegawa [abstract]), Sukegawa et al. teach the detection unit (Figure 12 element "4D", column 10 line 1-6) comprises an access memory for the at least one of the data processing units the access memory comprising locations for a plurality of the addresses that address locations in the memory units (Figure 15 element "10" "11A-C", column 11 line 23-53) that are addressable by the first one of the data processing units, the access memory being arranged to record access to the locations in the memory units (Figure 2A element "10", column 4 line 32-39), the detection unit being arranged to generate a detection signal indicating the new repetition in dependence (Column 11 line 45-53, column 13 line 17-24) on whether the access memory indicates that an address supplied by the first one of the processing units has been supplied before during the repetition.

As to claim 7, Humphrey et al. do not teach the detection unit generates the detection signal when the at least one of the data processing units outputs an address for which the access memory has previously recorded access after a previous detection

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of said new repetition. However, in the same field of data processing, Sukegawa et al. teach the detection unit generates the detection signal when the at least one of the data processing units outputs an address for which the access memory has previously recorded access after a previous detection of said new repetition (Figure 3, column 5 line 46-48).

As to claim 8, Humphrey et al. do not teach the detection unit generates the detection signal when the at least one of the data processing units has executed more than a certain number of addresses for which the access memory indicates that the address has not been supplied previously during the repetition (Figure 3, column 5 line 42-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Humphrey et al. and Sukegawa et al. because that would:

" Conventionally, because the host system must perform the address allocation management, the system without address allocation management software cannot handle such a memory system, thus leading to lack of universality as mentioned above." (Sukegawa, column 2 line 3-7)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dean Phan whose telephone number is (571) 270-1002. The examiner can normally be reached on Mon - Fri; 7:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Bruce can be reached on 571-272-2487. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DP



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